

Specification

TQM860M

TQM860M.SZ.102

27.11.2003


	Date:	Name:	Description:	Specification
Created:	27.11.2003	Frank Hattenhauer	Project:	TQM860M
Revised:	27.11.2003	Johannes Trepte	Document No.:	TQM860M.SZ.102
Company:			Release status	Checked
			Customer:	TQ-Components
File:	W:\Projekte\tqm860m\rev102\DOC\tqm860m.sz.102.doc			
<small>(C) TQ-Systems GmbH. All information contained in this document is strictly confidential. Disclosure of representations and information to third parties requires prior written consent of TQ-Systems GmbH.</small>				

Table of Contents

1. RANGE OF APPLICATION	5
2. SHORT DESCRIPTION	5
3. TECHNICAL CHARACTERISTICS	5
3.1 ELECTRONICS SPECIFICATION.....	5
3.1.1 Terms.....	5
3.1.2 Block Diagram.....	6
3.1.3 System Components.....	6
3.1.4 CPU.....	6
3.1.5 Supervisor.....	7
3.1.5.1 Tolerances and Reset Threshold for VCC3V3.....	7
3.1.5.2 Tolerances and Reset Threshold for VCC5V.....	7
3.1.5.3 Tolerances and Reset Threshold for VDDL.....	7
3.1.5.4 External Reset Input.....	8
3.1.6 Monitor Enable.....	8
3.1.6 Reset Configuration.....	8
3.1.7 Clock.....	9
3.1.7.1 CPU Clock.....	9
3.1.7.2 RTC Clock.....	10
3.1.7.3 CAN Clock.....	10
3.1.8 Driver for Reset Configuration Word.....	10
3.1.9 Bus Driver.....	11
3.1.10 Nonvolatile Memory (Flash).....	12
3.1.11 Dynamic Read/Write Memory (SDRAM).....	14
3.1.12 Serial EEPROM.....	15
3.1.13 CAN Controller.....	16
3.2 POWER SUPPLY.....	17
3.2.1 Possible Power Supplies.....	17
3.2.2 Core Supply VDDL.....	17
3.2.2.1 Current Consumption from VDDL.....	17
3.2.2.2 Switching Regulator for VDDL.....	18
3.2.3 3.3 V Supply.....	18
3.2.3.1 Current Consumption directly from 3.3 V.....	19
3.2.3.2 Total Consumption from 3.3 V.....	20
3.2.3.3 Switching Regulator for 3.3 V.....	20
3.2.4 5 V Supply.....	20
3.2.4.1 Current Consumption directly from 5 V.....	21
3.2.4.2 Total Consumption from 5 V.....	21
3.2.5 Battery Buffering.....	21
3.3 INTERFACES TO OTHER SYSTEMS AND DEVICES.....	21
3.3.1 Serial Interfaces.....	21
3.3.2 Download Interface.....	22
3.3.3 BDM interface.....	22
3.3.4 Module Connector.....	23
3.4 MECHANICS SPECIFICATION.....	29
3.4.1 General Information.....	29
3.4.2 Dimensions.....	29
3.4.3 Connector.....	31
3.4.4 Handling.....	31
3.5 MONITOR SOFTWARE.....	31
3.6 SAFETY REQUIREMENTS AND PROTECTIVE PROVISIONS.....	32
3.6.1 EMC Requirements.....	32
3.6.2 ESD Requirements.....	32
3.6.3 Operating Safety.....	32
3.7 ENVIRONMENTAL CONDITIONS.....	33
3.7.1 Climate and Operative Range.....	33

3.7.2	Mounting Conditions	33
3.8	RELIABILITY AND USEFUL LIFE.....	33
3.9	PRODUCT QUALIFICATION.....	33
3.9.1	Mechanical Strain.....	33
3.9.2	Temperature Tests.....	33
3.9.3	EMC	34
3.9.4	EMC Immunity.....	34
3.9.5	ESD	34
3.9.6	UL Approval.....	34
4.	APPENDIX.....	35
4.1	REFERENCES	35
4.2	CONFIGURATION OF SDRAMs	36
4.3	CONFIGURATION OF THE CAN CONTROLLERS	36

List of Illustrations:

Figure 1:	Block Diagram.....	6
Figure 2:	Tolerances of 3.3 V supply	7
Figure 3:	Tolerances of 5 V supply	7
Figure 4:	Tolerances of 1.8 V supply	8
Figure 5:	Configuration of Reset Configuration Word	11
Figure 6 :	Bus Structure	12
Figure 7:	Address multiplexing for SDRAMs.....	15
Figure 8 :	Mapping of the CAN controllers.....	16
Figure 9 :	Structure of Power Supply	17
Figure 10:	Driver Structure of RS232 Interfaces.....	22
Figure 11:	View from top through board	30
Figure 12:	Mounting Heights (not to scale)	30

List of Tables:

Table 1: Supported CPU derivatives5
 Table 2: Reset Configuration Word9
 Table 3: CPU clock10
 Table 4: RTC clock.....10
 Table 5: CAN clock10
 Table 6: Flash-Timing for 100 ns devices13
 Table 7: Flash-Timing for 120 ns devices13
 Table 8: Flash devices with 90 / 100 ns access time13
 Table 9: Flash devices with 110 / 120 ns access time13
 Table 10: Access timing with CL = 214
 Table 11: Access timing with CL = 314
 Table 12: Current consumption from VDDL.....17
 Table 13: 3.3 V supply specification18
 Table 14: Current consumption directly from 3.3 V.....19
 Table 15: Total current consumption directly from 3.3 V.....20
 Table 16: 5 V supply specification20
 Table 17: Current consumption directly from 5 V.....21
 Table 18: Total current consumption directly from 5 V.....21
 Table 19: VBAT supply specification21
 Table 20: Download Interface Signals.....22
 Table 21: BDM Interface Signals.....23
 Table 22: Module connector pinout29
 Table 23: Mounting Heights.....31
 Table 24: Connector types31

Modification index:

Rev.	Date:	It.	Name	Modification
101	18.08.2003		Trepte	Creation from detailed concept TQM860L.FK.356 and TQM860L specification TQM860L.SZ.301B
102	12.11.2003		Hattenhauer	New flash types added (section 3.1.10); switching regulator for VCC3V3 with max. 1500 mA output (section 3.2.3); alternative clock generation for 66 MHz with PLL (section 3.1.7.1)

1. Range of Application

The present document describes the technical characteristics of various microcontroller modules of the TQM8xxL series. The designation MPC860 is mostly used synonymously for all microcontrollers of the MPC8xx series (see Table 1) that can be used. Also, in most cases, TQM860M stands for the following variants:

Product Key	CPU
TQM860M.....-x freq.101	MPC860 and variants (x = DE, DP, DT, EN, P, SR, T)
TQM862M.....-T freq.101	MPC855T
TQM862M.....-x freq.101	MPC862 and variants (x = T, P)
TQM857M.....-x freq.101	MPC857 and variants (x = T, DSL)
TQM866M.....-x freq.101	MPC866 and variants (x = T, P)
TQM859M.....-x freq.101	MPC859 and variants (x = T, DSL)

Table 1: Supported CPU derivatives

The product key will be explained in a separate document.

2. Short Description

TQM860M is a universal minimodule with the PowerPC-CPU MPC860 by Motorola. The pin assignment of all modules of the TQM8xxM and TQM8xxL series is compatible, i.e. the pins of the TQM860M are a set including subsets of pins of the TQM850L and future TQM850M. This allows modules with different performance and different interfaces to be used in the same base board as required.

All relevant pins of the microprocessor and in particular all port pins are led through onto the connectors. This keeps the system more transparent for the developer of the base board, and the potential of the hardware can be fully exhausted.

3. Technical Characteristics

3.1 Electronics Specification

3.1.1 Terms

The following terms and abbreviations will be used:

BDM	Background Debug Mode
CPU	Central Processing Unit
EEPROM	Electrically erasable programmable read-only memory (bitwise re-writable)
EMC	Electromagnetic Compatibility
Flash	Electrically erasable programmable read-only memory (block erase)
JTAG	Joint Test Action Group
MCU	Memory Control Unit
RTC	Real Time Clock
SDRAM	Synchronous Dynamic Random Access Memory
SMD	Surface Mounted Device

Specification TQM860M

3.1.2 Block Diagram

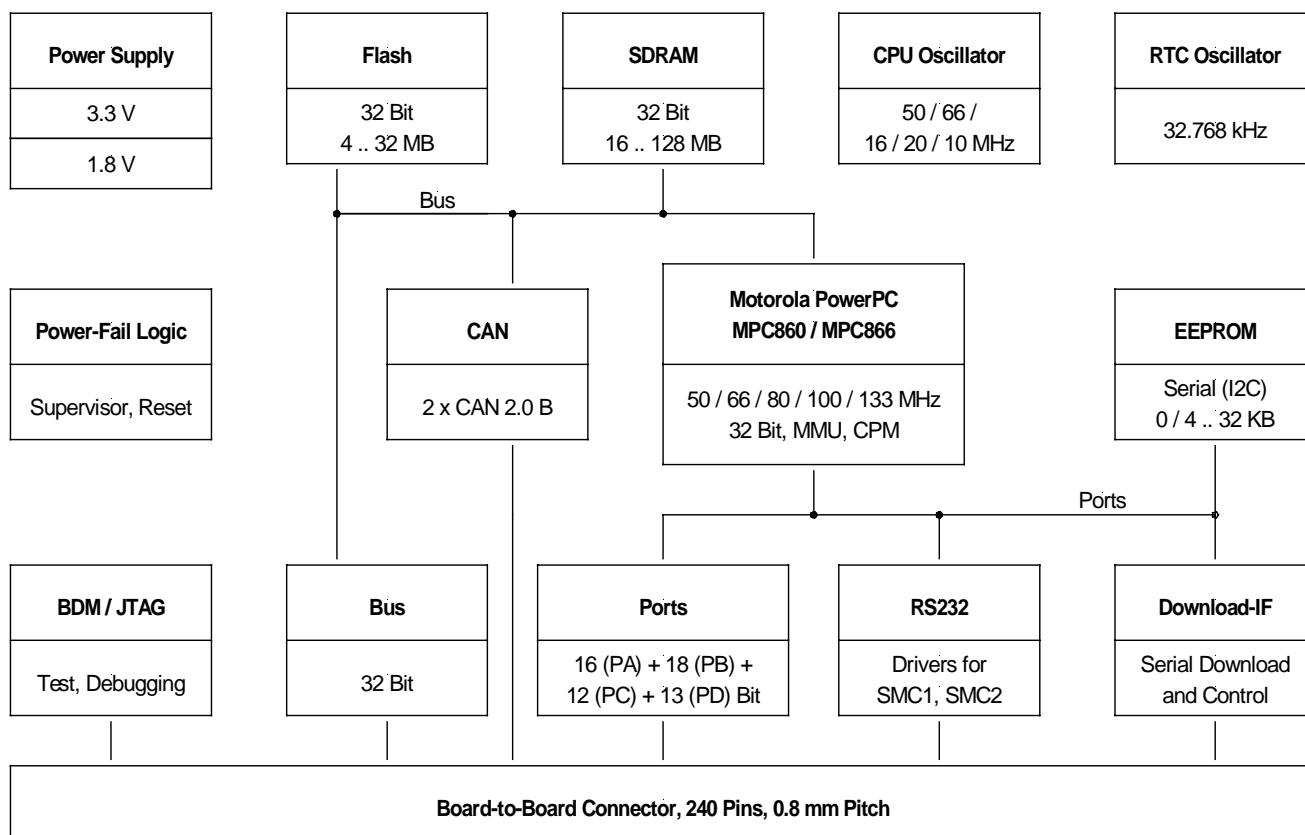


Figure 1: Block Diagram

3.1.3 System Components

- CPUs MPC860 and derivatives
- Oscillator for CPU
- Oscillator for RTC
- Power fail logic
- Switching regulators
- SDRAM, Flash
- 2 * Full CAN 2.0 B active
- 2 * RS232 serial driver for SMC1 and SMC2
- BDM interface
- 0.8 mm pitch board-to-board connector system, 240 pins

3.1.4 CPU

The module was developed for the MPC860 but can also be used for an MPC855 and other derivatives (see 1.). Subject to an adequate product qualification, future derivatives can be deployed, provided their pins and functions are compatible to the MPC860.

The addresses for driving the SDRAMs are internally multiplexed. Therefore it is not possible to access SDRAM by an external bus master (e.g. PCI Bridge, multiprocessor system).

Specification TQM860M

3.1.5 Supervisor

3.1.5.1 Tolerances and Reset Threshold for VCC3V3

Tolerance for external supply (see Figure 2, Pos. A):
 $V_{CC3V3} = 3.3 \text{ V} - 3.18 \% / + 5 \% = 3.195 \text{ V} \dots 3.465 \text{ V}$

Tolerance of internal supply / switching regulator (see Figure 2, Pos. B):
 $V_{CC3V3} = 3.287 \text{ V} \pm 3.1 \% = 3.185 \text{ V} \dots 3.392 \text{ V}$ (standard and extended temperature range)

Permissible operating range, CPU and 3.3 V logic (see Figure 2, Pos. C):
 $V_{CC3V3} = 3.3 \text{ V} \pm 5 \% = 3.135 \text{ V} \dots 3.465 \text{ V}$

Tolerance of supervisory circuit (extended temperature range, LM4050 / LMC7221):
 $V_{Reset} = 3.135 \dots 3.178 \text{ V}$

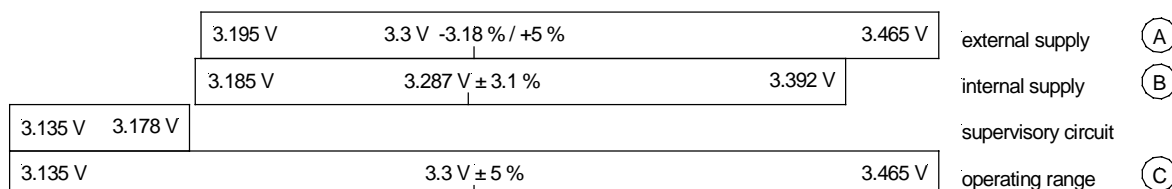


Figure 2: Tolerances of 3.3 V supply

3.1.5.2 Tolerances and Reset Threshold for VCC5V

Supply tolerance (see Figure 3, Pos. D):
 $V_{CC5V} = 5 \text{ V} - 8.6 \% / + 10 \% = 4.57 \text{ V} \dots 5.5 \text{ V}$

Permissible operating range, CAN controller and 5 V logic (see Figure 3, Pos. E):
 $V_{CC5V} = 5 \text{ V} \pm 10 \% = 4.5 \text{ V} \dots 5.5 \text{ V}$

Tolerance of supervisory circuit:
 $V_{Reset} = 4.50 \text{ V} \dots 4.57 \text{ V}$ (extended temperature range, LM4050 / LMC7221)

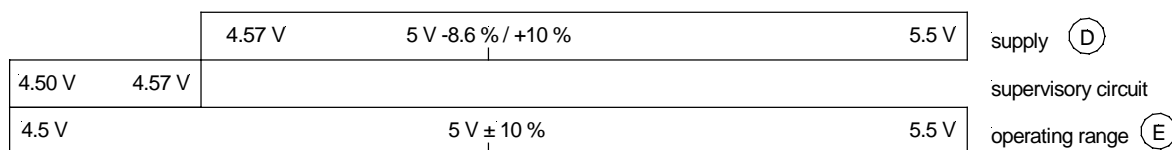


Figure 3: Tolerances of 5 V supply

3.1.5.3 Tolerances and Reset Threshold for VDDL

Tolerance of internal supply / switching regulator (see Figure 4, Pos. F):
 $V_{DDL} = 1.8 \text{ V} \pm 2.8 \% = 1.752 \text{ V} \dots 1.853 \text{ V}$ (standard and extended temperature range)

Permissible operating range, CPU-Core (see Figure 4, Pos. G):
 $V_{DDL} = 1.8 \text{ V} \pm 5 \% = 1.7 \text{ V} \dots 1.9 \text{ V}$

Tolerance of supervisory circuit (extended temperature range, LM4050 / LMC7221):
 $V_{Reset} = 1.705 \text{ V} \dots 1.732 \text{ V}$

Specification TQM860M

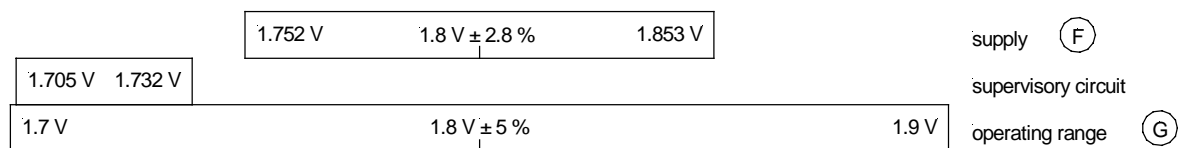


Figure 4: Tolerances of 1.8 V supply

3.1.5.4 External Reset Input

With the signal RESIN#, a debounced, low-active reset input is provided. The RESIN# signal is provided with a pull-up resistor and thus can be driven by either a push-pull or open-collector output. The minimum required low level is 0.6 V.

3.1.6 Monitor Enable

A switching circuitry connects the ENMON# signal to the CPU's PA15 pin for approx. 30 ms after a reset. After that, the circuit re-connects the CPU's PA15 signal to the module connector. Like the CPU's PA15 pin, both ENMON# and PA15 at the module connector are 5 V tolerant.

3.1.6 Reset Configuration

Usually, the system reads the reset configuration from the bus (RSTCONF# = 0). If required, however, the default configuration (RSTCONF# = 1 → bits 0 .. 15 = 0) can also be used by applying a high level to RSTCONF#.

Bits	Name	Description	50 / 66 MHz	80 / 100 / 133 MHz
0	EARB	External arbitration. If this bit is set, external arbitration is assumed. If it is cleared, internal arbitration is performed.	0	0
1	IIP	Initial interrupt prefix. Defines the initial value of the MSR[IP] which defines the interrupt table location. If IIP is cleared (default), the MSR[IP] initial value is one; if it is set, the MSR[IP] initial value is zero.	1	1
2	BBE	Boot Burst Enable 0 The boot device does not support bursting. 1 The boot device does support bursting.	0	0
3	BDIS	Boot disable. If BDIS is set, memory bank 0 is invalid; that is, BR0[V] is cleared. 0 The memory controller is activated after reset so that it matches all addresses. 1 The memory controller is cleared after reset but is not activated.	0	0
4–5	BPS	Boot port size. Defines the port size of the boot device as shown in the following chart. 00 32-bit port size. 01 8-bit port size. 10 16-bit port size. 11 Reserved.	00	00
6	–	Reserved for future use and should be allowed to float.	0	0
7–8	ISB	Initial internal space base select. Defines the initial value of the IMMR bits 0-15 and determines the base address of the internal memory space.	11	11

Specification TQM860M

Bits	Name	Description	50 / 66 MHz	80 / 100 / 133 MHz
		00 0x00000000. 01 0x00F00000. 10 0xFF000000. 11 0xFFFF00000.		
9–10	DBGC	Debug pin configuration. See 4.1 for details.	11	11
11–12	DPPC	Debug port pins configuration. See 4.1 for details. Configuration for BDM-Debugging (JTAG/BDM# = 1 or open) Configuration for JTAG-Test (JTAG/BDM# = 0)	01 / 00*	01 / 00*
13–14	EBDF	External bus division factor. Defines the frequency division factor between GCLK1/GCLK2 and GCLK1_50/GCLK2_50. CLKOUT is similar to GCLK2_50. GCLK2_50 and GCLK1_50 are used by the system interface unit and memory controller to interface with the external system. 00 Full speed bus 01 Half speed bus 10 Reserved 11 Reserved	00	01
15	CLES	Core Little Endian Swap. Defines core access operation following reset. 0 Big Endian 1 Little Endian	0	0

* Depends on JTAG/BDM# signal

Table 2: Reset Configuration Word

3.1.7 Clock

3.1.7.1 CPU Clock

The central clock signal of the module is CLKOUT (= external bus clock). The overall timing of the MPC860 is synchronous to this signal. It is also used for addressing the SDRAMs and led onto the module connectors.

The CLKOUT signal is buffered by a zero-delay buffer. On the module itself, buffered clocks and a point-to-point clock routing is used to obtain best possible signal quality. By choosing fitting variants, the CLKOUT signal can be connected the modul connectors either unbuffered or buffered. The standard variant with buffered CLKOUT prevents an interference of the external circuitry to the module, and externally the full driver power of 50 pF can be used.

The CPU clock is generated with an oscillator and multiplied if required. For the MPC860 and derivatives, the necessary settings are made without involvement of the software via the reset configuration word. For the MPC866 and derivatives, the PLL is re-configured by software. For details see [22].

The tolerances include the output tolerance as well as changes in frequency caused by temperature, changes in supply voltage, ageing, shock and vibration.

Clock rate CPU [MHz]	Oscillator frequency [MHz]	Multiplication factor CPU	MODCK1:2	Divisor factor ext. bus	Clock rate ext. bus [MHz]
50 ± 100 ppm	50 ± 100 ppm	1	10	1	50 ± 100 ppm

Specification TQM860M

Clock rate CPU [MHz]	Oscillator frequency [MHz]	Multiplication factor CPU	MODCK1:2	Divisor factor ext. bus	Clock rate ext. bus [MHz]
66 ± 100 ppm	66 ± 100 ppm	1	10	1	66 ± 100 ppm
66 ± 100 ppm	13.2 ± 100 ppm	5	10	1	66 ± 100 ppm
80 ± 100 ppm	16 ± 100 ppm	5	11	2	40 ± 100 ppm
100 ± 100 ppm	20 ± 100 ppm	5	11	2	50 ± 100 ppm
133 ± 100 ppm	10 ± 100 ppm	13.3	11	2	66.5 ± 100 ppm

Table 3: CPU clock

3.1.7.2 RTC Clock

The oscillator integrated in the CPU generates the RTC clock of 32.768 kHz with the aid of an external quartz crystal. This clock is used for running the integrated RTC. When starting the MON8xx, it is used as reference clock in order to determine the clock rate of the CPU.

Tolerance of the RTC frequency:

Rated frequency	Output tolerance	Temperature coefficient max.	Ageing max.	Change in frequency by shock max.
32.768 kHz	± 50 ppm	-0.04 ppm / °C ²	± 3 ppm / a	± 5 ppm

Table 4: RTC clock

Note:

In some CPU variants and masks, an error in the CPU leads to a considerably increased current consumption from VBAT when the main supply is switched off. For more information see the relevant Errata Sheets of Motorola.

3.1.7.3 CAN Clock

The on-chip oscillator of the first CAN controller generates a clock of 16 MHz with the aid of an external quartz. The second controller receives its clock from the CLKOUT of the first. This has to be taken into account when initializing the CAN controllers. From their respective clocks, the CAN controllers generate the baud rates for the CAN bus.

Tolerance of the CAN clock:

Rated frequency	Output tolerance	Temperature stability	Ageing max.
16 MHz	± 50 ppm	± 120 ppm	± 5 ppm / a

Table 5: CAN clock

3.1.8 Driver for Reset Configuration Word

Bits 0 to 15 of the Reset Configuration Word are implemented completely via an active driver – i.e., both high and low bits are driven. This is to avoid possible problems following changes to the CPU-internal pull-ups (e.g., new mask or technology from Motorola).

Bits 16 to 31 are not included in the driver. They are not used with the current MPC8xx CPUs.

Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Field	EARB	IIP	BBE	BDIS	BPS	—	—	ISB	—	DBGC	—	DBPC	—	EBDF	—	CLES
Default	0000_0000_0000_0000															
Bit	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Field	—															
Default	0000_0000_0000_0000															

NOTE: The default value is due to the internal pull-down resistor on the data bus.

Figure 5: Configuration of Reset Configuration Word

In Figure 5, the previously configured bits (could be set to 1 on TQM860L.300) are shown white, the new bits gray. Of the gray bits, dark-gray represents an extension of the Reset Configuration Word by Motorola (maximum current usage on MPC855T), and the light-gray bits were already used on MPC860 and are now only actively driven with a low level. Since an 18-bit driver has to be used anyway for the required 17 bits, the remaining driver is used for the reserved bit 6.

3.1.9 Bus Driver

- No buffering of the address line on the module: SDRAM and flash are driven without additional delay.
- Unbuffered address bus led through: External periphery can only be connected by pre-connecting a driver. The necessary load capacity for a driver input is still available (see 3.3.4).
- Data bus led through unbuffered: Direct connection up to ca. 20 pF possible (see 3.3.4). For higher bus loads, external buffers are required.

Due to the complete configuration of all bits used in the Reset Configuration Word (see 3.1.8), buffers with “bus hold” can be used on baseboards.

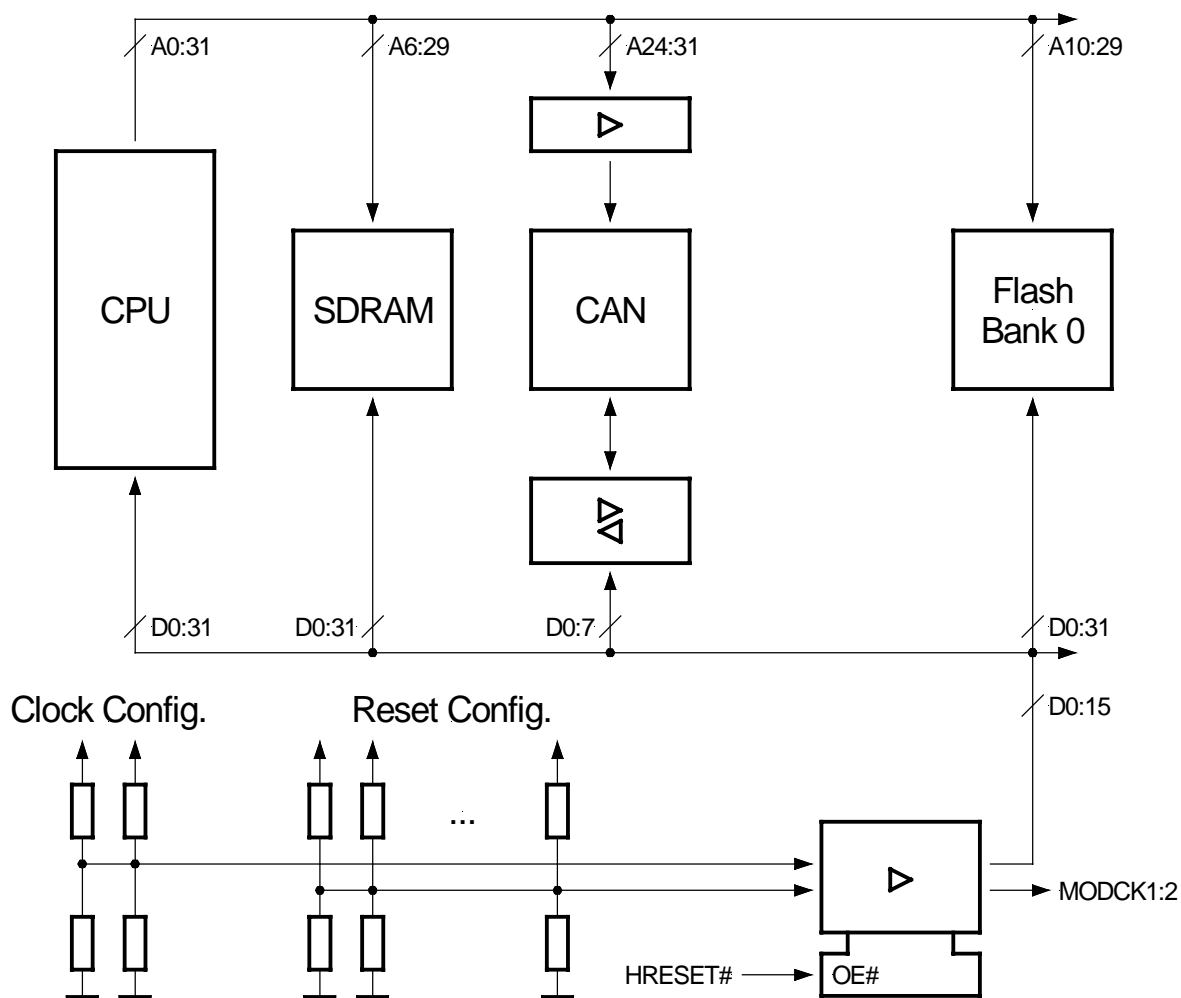


Figure 6 : Bus Structure

3.1.10 Nonvolatile Memory (Flash)

16-bit wide 3.3 V flashes in a BGA package are used. They are addressed directly by the CPU without driver / buffer.

- 4 to 32 MB
- 1 bank of 32 bit width
- Device access time 100 or 120 ns
- Signals used:
CS_FLASH0#/CS0# (bootable) and CS_FLASH1#/CS1# if req.,
OE#/GPL_AB1#, WE0#/BS_B0#, WE2#/BS_B2#
- Addressing via GPCM, recommended timing see below

Specification TQM860M

Access type	Bus clock [MHz]	CSNT	ACS	SCY	TRLX	EHTR
Boot read	50 / 66 / 40	1	11b	15	1	0
Normal Read / Write	50		00b	2		0
	66			3		
	40			3		

Table 6: Flash-Timing for 100 ns devices

Access type	Bus clock [MHz]	CSNT	ACS	SCY	TRLX	EHTR
Boot read	50 / 66 / 40	1	11b	15	1	0
Normal Read / Write	50		00b	3		0
	66			4		
	40			4		

Table 7: Flash-Timing for 120 ns devices

The status signal RY/BY# of the flashes is not used, i. e. the sequence of the write and delete cycles has to be monitored by polling the flash status bits (DQ7#, toggle bits, etc.) [4].

Since each of the two 16 bit wide flashes of a 32 bit bank only has one write enable signal, only 16 or 32 bit wide writing (programming) is possible. Individual bytes can be programmed as follows:

1. Read out the word from the flash containing the byte you want to program
2. In the retrieved word, replace the byte you want to program
3. Write back the data word

The following devices are used:

Component (Access Time)	Manufacturer	Type	Ext. Temp.	Alternative Manufacturer
Am29LV160MB-90PCC (90 ns)	AMD	1M * 16 (2M * 8) FBGA64 13 x 11	possible -PCI	
Am29DL163DB-90PCI (90 ns)	AMD	1M * 16 (2M * 8) FBGA64 13 x 11	YES	
Am29LV320ML-90RPCI (90 ns)	AMD	2M * 16 (4M * 8) FBGA64 13 x 11	Yes	
Am29LV640ML-90RPCI (90 ns)	AMD	4M * 16 (8M * 8) FBGA64 13 x 11	Yes	Fujitsu MBM29LP650ULM90PBT
Am29LV128ML-93RPCI (90 ns)	AMD	8M * 16 (16M * 8) FBGA64 13 x 11	Yes	

Table 8: Flash devices with 90 / 100 ns access time

Component (Access Time)	Manufacturer	Type	Ext. Temp.	Alternative Manufacturer
Am29LV320ML-112RPCI (110 ns)	AMD	2M * 16 (4M * 8) FBGA64 13 x 11	Yes	
Am29LV320MB-110RPCI (110 ns)	AMD	2M * 16 (4M * 8) FBGA64 13 x 11	Yes	
Am29LV640ML-112RPCI (110 ns)	AMD	4M * 16 (8M * 8) FBGA64 13 x 11	Yes	
Am29LV128ML-113RPCI (110 ns)	AMD	8M * 16 (16M * 8) FBGA64 13 x 11	Yes	

Table 9: Flash devices with 110 / 120 ns access time

Specification TQM860M

NOTE:

For some of the listed types, the driver power is specified with 30 pF. According to AMD technical support, they can be used with 50 pF load, if a delay of 2 ns is added to access times.

Due to different sector alignment the flash types AM29DL163DB and AM29LV320MB are not supported by the current MON8xx monitor version 110.

3.1.11 Dynamic Read/Write Memory (SDRAM)

As SDRAM memory, 16-bit wide SDRAM components are used in the TSSOP54 package.

- 16 to 128 MB
- 1 memory bank of 32-bit width
- Clock 50 MHz (50 and 100 MHz module), 66 MHz (66 and 133 MHz module), or 40 MHz (80-MHz module)
- Signals used:
 - CS_SDRAM0#/CS2#
 - GPL_AB0# (A10 SDRAM)
 - OE#/GPL_AB1# (WE# SDRAM)
 - GPL_AB2# (RAS# SDRAM)
 - GPL_AB3# (CAS# SDRAM)
 - BS_A0# (DQMU SDRAM, Bits 0 .. 7)
 - BS_A1# (DQML SDRAM, Bits 8 .. 15)
 - BS_A2# (DQMU SDRAM, Bits 16 .. 23)
 - BS_A3# (DQML SDRAM, Bits 24 .. 31)
 - CLKOUT
 - CKE (only provided with pull-up)
- Addressing and refresh via UPMA
- CAS latency 2 or 3 (different UPM patterns)

Depending on the memory configuration, 2 chips of 64, 128, 256 or 512 MBit are used. Note that “monolithic” types should be used – i.e., not multi-chip types, since these present a much higher bus load. Currently, 512 MBit SDRAMs are only available with CAS latency 3. The variant dependent choice of address lines is implemented by optionally fitted 0-Ω resistors.

The following access scheme is recommended (see appendix 4):

CLKOUT	Single Read	Burst Read	Single Write	Burst Write	SDRAM type
66 MHz	4 + 1	4 + 1 + 1 + 1 + 1	3 + 1	3 + 1 + 1 + 1 + 1	PC133
50 MHz	4 + 1	4 + 1 + 1 + 1 + 1	3 + 1	3 + 1 + 1 + 1 + 1	PC100
40 MHz	4 + 1	4 + 1 + 1 + 1 + 1	3 + 1	3 + 1 + 1 + 1 + 1	PC100

Table 10: Access timing with CL = 2

CLKOUT	Single Read	Burst Read	Single Write	Burst Write	SDRAM type
66 MHz	5 + 1	5 + 1 + 1 + 1 + 1	3 + 1	3 + 1 + 1 + 1 + 1	PC133
50 MHz	5 + 1	5 + 1 + 1 + 1 + 1	3 + 1	3 + 1 + 1 + 1 + 1	PC100
40 MHz	5 + 1	5 + 1 + 1 + 1 + 1	3 + 1	3 + 1 + 1 + 1 + 1	PC100

Table 11: Access timing with CL = 3

Specification TQM860M

The configuration of address lines according to SDRAM type is implemented as follows:

Hardwired

CPU-internally multiplexed

64 MBit

SDRAM	BA1	BA0	NC	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
mux	8	9	7	10	11*	12	13	14	15	16	17	18	19	20	21
non-mux	8	9	7	18	AP	20	21	22	23	24	25	26	27	28	29

128 MBit

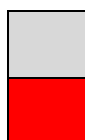
SDRAM	BA1	BA0	NC	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
mux	8	7	7	9	10	11	12	13	14	15	16	17	18	19	20
non-mux	8	7	7	18	AP	20	21	22	23	24	25	26	27	28	29

256 MBit

SDRAM	BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
mux	8	6	7	9	10	11	12	13	14	15	16	17	18	19	20
non-mux	8	6	7	18	AP	20	21	22	23	24	25	26	27	28	29

512 MBit

SDRAM	BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
mux	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
non-mux	5	6	7	18	AP	20	21	22	23	24	25	26	27	28	29



Gray: Don't care

Red: Modifications since Rev. 300

Figure 7: Address multiplexing for SDRAMs

3.1.12 Serial EEPROM

An additional I²C-EEPROM was integrated on the module. Unlike the flash, individual memory cells of the EEPROM can be deleted and re-written. The delivered EEPROM is empty. It can store e.g. configuration data in a nonvolatile manner.

Specification TQM860M

As the smallest package, which can be supplied by several manufacturers, TSSOP-8 was chosen. In order to maintain software-compatibility to the existing TQM8260.200 (manufacturer, memory capacity, addresses), all address inputs were set to low. For all variants with a fitted EEPROM, pull-ups are provided for at I2CSCL and I2CSDA.

- 0 to 32 KB
- Addressing via I²C bus of the CPU (I2CSCL / I2CSDA)

3.1.13 CAN Controller

One or two AS82527 (Intel) are used. These are addressed by the CPU via drivers (addresses, chip select) and buffers (data).

- Two full CAN 2.0b compatible interfaces
- No CAN transceivers (input and output at TTL level)
- Clock from common 16 MHz quartz crystal connected to the first controller, CLKOUT of the first controller is led onto XTAL1 of the second
- Access mode 8 bit non-multiplexed
- Signals used:
 - CS_CAN#/CS3#
 - GPL_AB2# (R/W# CAN)
 - GPL_A5# (buffer enable bus transceiver for CAN)
 - A22, A23 (address decoding)
 - HRESET# (RESET# CAN)
 - IRQ_CAN#/IRQ4# (common interrupt for CAN)
- addressing via UPMB, adaptive timing (wait signal)

Recommended setup: See appendix 0

The resulting mapping in relation to the base address of CS_CAN#/CS3# hence looks like shown in Figure 8. The area shown is mirrored to the offsets +0x400, +0x800 etc. Access to the area 0x200 to 0x3FF and its reflections lead to a bus timeout and should be avoided.

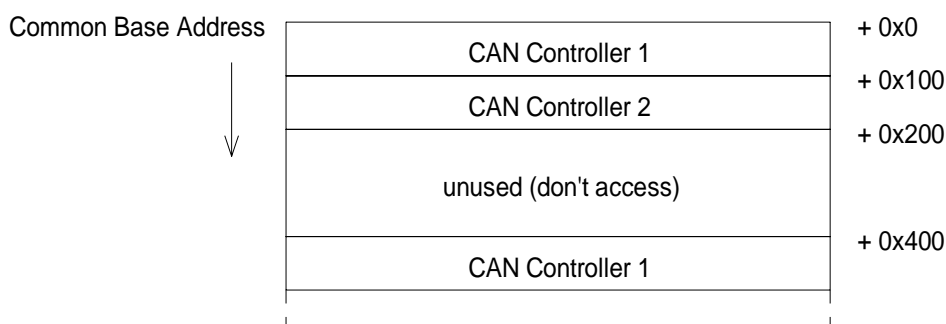


Figure 8 : Mapping of the CAN controllers

3.2 Power supply

3.2.1 Possible Power Supplies

The power supply of the module is structured as follows:

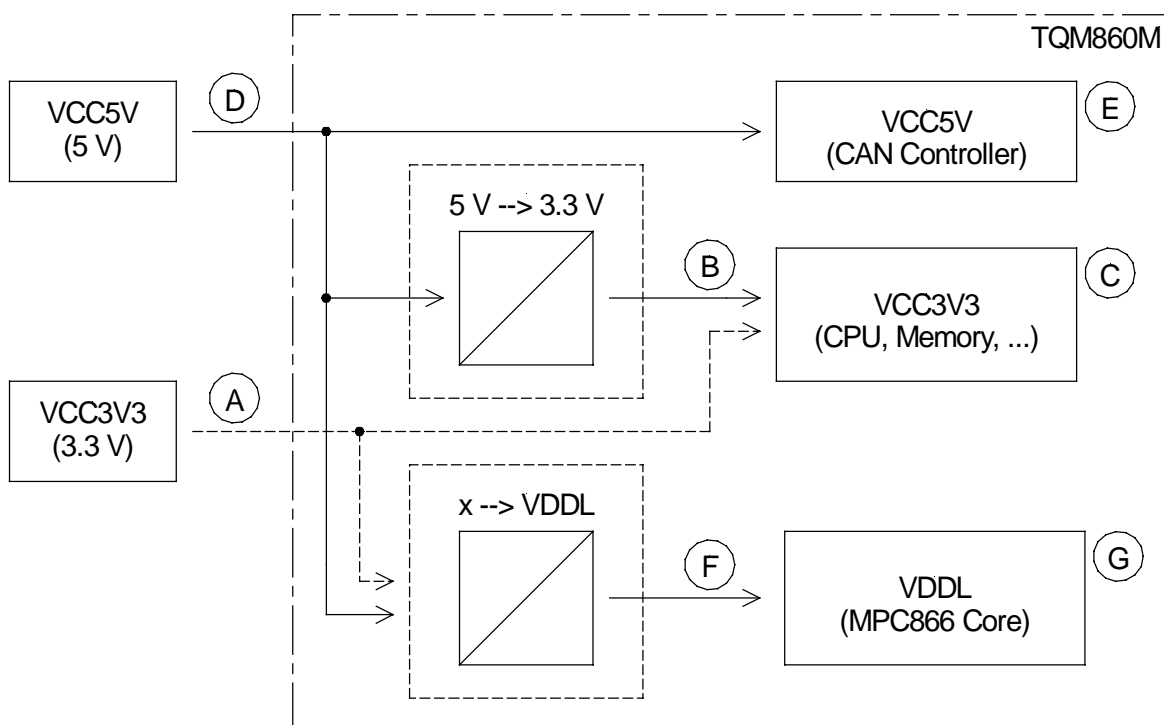


Figure 9 : Structure of Power Supply

Depending on the module variant, the following possibilities for supplying the module with power arise:

- With CAN controller: Input voltage 5 V or 5 V and 3.3 V separately
- Without CAN controller: Input voltage 5 V or 3.3 V

For a 5-V-only supply, a step-down switching regulator from 5 V to 3.3 V is used.

3.2.2 Core Supply VDDL

3.2.2.1 Current Consumption from VDDL

Component	Type	Current consumption @ 133 MHz max. [mA]
CPU Core	MPC866 [7]	178

Table 12: Current consumption from VDDL

All specifications refer to a worst-case situation.

Specification TQM860M

3.2.2.2 Switching Regulator for VDDL

This option has to be chosen whenever a MPC866 series CPU is used. VDDL is created either from 5 V (if the switching regulator from 5 V to 3.3 V is present), or from 3.3 V.

- Conversion 5 V or 3.3 V → 1.8 V
- $I_{out(max)} = 250 \text{ mA}$
- Synchronous rectification / high efficiency
- High switching frequency (> 200 kHz → small components)
- Ceramic input and output capacitors

Used components:

Component	Manufacturer	Type	Ext. Temp.	Alternative Manufacturer
TPS40003	Texas Instruments	Switching regulator, 600 kHz	Yes	no
FDC6305N	Fairchild	Dual N-MOSFET SOT23-6	Yes	Vishay
Si3900DV	Vishay	Dual N-MOSFET SOT23-6	Yes	Fairchild
744 551 0	Würth	10 μH , 1,1 A 160 $\text{m}\Omega$		

3.2.3 3.3 V Supply

Voltage VCC3V3 (external supply)	3.195 .. 3.465 V	Determined by voltage range of components and supervisor threshold (see 3.1.5.1)
Ripple max.	40 mV	peak – peak
Output current switching regulator max.	1500 mA	guaranteed output current (worst case)
Extractable current	–	no extraction provided for external load

Table 13: 3.3 V supply specification

Specification TQM860M

3.2.3.1 Current Consumption directly from 3.3 V

Component	Type	Current consumption max. [mA]				
		50 MHz	66 MHz	80 MHz	100 MHz	133 MHz
CPU	MPC860 [5] [6] / MPC866 [7]	231	265	275	461	161
FLASH	2 * 29LVxxxM (write) [8]	120	120	120	120	120
SDRAM	2 * MT48LC16M16A2TG-75 (160 mA, cont. burst, all banks active @ 100 MHz [9])	160	211	128	160	211
EEPROM		3	3	3	3	3
RS232	MAX3222CAP (115 kBaud, 3 kΩ / 1000 pF), 2 * I _{type} [14]	25	25	25	25	25
Watchdog	(Ref., Comparators, Supervisor)	≅ 0	≅ 0	≅ 0	≅ 0	≅ 0
Gen. logic	(Reset Config., CAN)	15	15	15	15	15
Total		554	639	566	784	535

Table 14: Current consumption directly from 3.3 V

All specifications refer to a worst-case situation.

The switching regulator should be equipped for at least 800 mA. Future variants with 133 MHz are not taken into account since these will have a separate core supply at a lower voltage.

Consumption estimates in detail:

- CPU:

The worst case to date is a 66 MHz CPU with 66 MHz bus clock. The redesign takes account of a 100 MHz CPU / 50 MHz bus. The estimate for this is based on the 50 MHz / 50 MHz module.

For the MPC866 series, the following estimation is made for I/O power consumption:

$$I_D = 70 \text{ (no. of drivers)} * 35 \text{ pF (C}_{\text{Load}}) * 3.3 \text{ V} * 66.5 \text{ MHz (bus clock)} * 0.5 \text{ (average level change rate per clock)} * 0.6 \text{ (average number of driven signals)} = 161 \text{ mA}$$

- EEPROM [10][11]:

$$\Delta I_{CC} = I_{CC} = 3 \text{ mA (write, 400 kHz)}$$

- Flash [8]:

$$I_{CC4} = 60 \text{ mA (write)} * 2 = 120 \text{ mA}$$

All data apply to the worst case.

Specification TQM860M

3.2.3.2 Total Consumption from 3.3 V

If the module is supplied from 3.3 V only, the input current of the switching regulator supplying the core is added to the current drawn directly from 3.3 V (MPC866 series CPU only).

Component	Type	Current consumption max. [mA]				
		50 MHz	66 MHz	80 MHz	100 MHz	133 MHz
3.3 V Logic	see 3.2.3.1	554	639	566	784	535
Switching regulator for VDDL	Input current = consumption 1.8 V * (1.8 / 3.3) / eta (0.90)	–	–	–	–	108
Total		556	619	565	724	643

Table 15: Total current consumption directly from 3.3 V

3.2.3.3 Switching Regulator for 3.3 V

This option has to be chosen whenever no external 3.3 V supply of the module is available. From the external supply (5 V), a step-down switching regulator creates the operating voltage of 3.3 V to supply the CPU and all other 3.3 V components.

- Conversion 5 V → 3.3 V
- $I_{out(max)} = 1000$ mA (dimensioning only for module, no external load admissible)
- Synchronous rectification / high efficiency
- High switching frequency (> 200 kHz → small components)
- Ceramic input and output capacitors

Used components:

Component	Manufacturer	Type	Ext. Temp.	Alternative Manufacturer
TPS40003	Texas Instruments	Switching regulator, 600 kHz	Yes	no
FDC6305N	Fairchild	Dual N-MOSFET SOT23-6	Yes	
744 550 33	Würth	3.3 μH, 2 A, 80 mΩ		

3.2.4 5 V Supply

Voltage VCC5V (with CAN controller)	4.590 .. 5.5 V	Determined by voltage range of components and supervisor threshold (see 3.1.5.2)
Voltage VCC5V (without CAN controller)	4.5 .. 5.5 V	Determined by design of the switching regulator
Ripple max.	60 mV	peak – peak

Table 16: 5 V supply specification

Specification TQM860M

3.2.4.1 Current Consumption directly from 5 V

Component	Type	Current consumption max. [mA]
CAN Controller	2 * AS82527 [10]	100
gen. logic		≅ 50
Total		150

Table 17: Current consumption directly from 5 V

3.2.4.2 Total Consumption from 5 V

If the module is supplied from 5 V only, the input current of the switching regulator supplying the 3.3 V logic is added to the current drawn directly from 5 V:

Component	Type	Current consumption max. [mA]				
		50 MHz	66 MHz	80 MHz	100 MHz	133 MHz
5 V Logic	see 3.2.4.1	150	150	150	150	150
Switching regulator for 3.3 V	Input current = consumption 3.3 V * (3.3 / 5) / eta (0.90)	406	469	415	574	392
Switching regulator for VDDL	Input current = consumption 1.8 V * (1.8 / 5) / eta (0.90)	–	–	–	–	71
Total		556	619	565	724	613

Table 18: Total current consumption directly from 5 V

3.2.5 Battery Buffering

Buffering of the RTC integrated in the CPU is provided for in the design.

Voltage VBAT	2.0 .. 3.6 V	
Current consumption	10 µA 20 mA*	Maximum value (worst case) Maximum value (with CPU error G2)

* The value applies to CPUs with the “RTC bug” referred to as "G2" by Motorola Errata Sheets, e.g. MPC860 up to and including C1 mask. For information about current mask status see Errata Sheets of Motorola.

Table 19: VBAT supply specification

3.3 Interfaces to Other Systems and Devices

3.3.1 Serial Interfaces

- Two internal UARTs

Specification TQM860M

- Max. 115200 baud
- Driver with RS232 compatible levels
- All signals also available without driver
- Standard equipping driver 2 * RxD / TxD

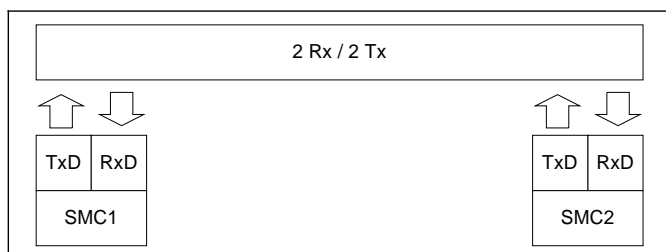


Figure 10: Driver Structure of RS232 Interfaces

3.3.2 Download Interface

- RxD and TxD
- Reset via RS232 interface (RESIN#)
- additional input line from RS232 (ENMON#, can be addressed via port pin)

The download interface is an extension of the serial interface for control purposes. It consists of five signals which are merely present on the connectors to the base board. On the starter kit STK8xxL, they are combined with the connector for SMC1.

Pin*	Signal name	Type	Function
6	ENMON#	I	Switch monitor / normal boot process
3	SMTXD1	O	TxD of debugging interface (SMC1, RS232 level)
5	GND	–	Ground
1	RESIN#	I	Reset input (master reset of reset component)
2	SMRXD1	I	RxD of debugging interface (SMC1, RS232 level)

* on starter kit STK8xxL

Table 20: Download Interface Signals

3.3.3 BDM interface

All lines of the Motorola BDM interface (debugging interface) are provided outwardly. Like the download interface, the BDM interface is exclusively led onto the connectors to the base board. It comprises the following signals:

Pin*	Signal name	Type	Function
1	FRZ# (VFSL0)**	O	Freeze (CPU history buffer status)
2	SRESET#	I/O	Soft reset
3	DGND	–	Ground
4	DSCK/TCK	I	Clock
5	DGND	–	Ground
6	FRZ# (VFSL1)**	O	Freeze (CPU history buffer status)
7	HRESET#	I/O	Hard reset

Pin*	Signal name	Type	Function
8	DSDI/TDI	I	Data input
9	VCC3V3	–	Power supply
10	DSDO/TDO	O	Data output

Table 21: BDM Interface Signals

* on starter kit STK8xxL

** alternative assignment in brackets

3.3.4 Module Connector

- 32 Bit data bus
- 32 bit address bus
- All port I/O pins

Signal	No. of Pins	Type	Description	Ext. Load Cap. max. [pF]	Module Pin
--------	-------------	------	-------------	--------------------------	------------

Address Bus

A0	B19	I/O, TS	Address A0 (MSB)	50	X1-111
A1	B18	I/O, TS	Address A1	50	X1-110
A2	A18	I/O, TS	Address A2	50	X1-109
A3	C16	I/O, TS	Address A3	50	X1-108
A4	B17	I/O, TS	Address A4	50	X1-107
A5	A17	I/O, TS	Address A5	50	X1-106
A6	B16	I/O, TS	Address A6	40	X1-105
A7	A16	I/O, TS	Address A7	40	X1-104
A8	D15	I/O, TS	Address A8	10	X1-103
A9	C15	I/O, TS	Address A9	10	X1-102
A10	B15	I/O, TS	Address A10	10	X1-101
A11	A15	I/O, TS	Address A11	20	X1-100
A12	C14	I/O, TS	Address A12	20	X1-99
A13	B14	I/O, TS	Address A13	20	X1-98
A14	A14	I/O, TS	Address A14	20	X1-97
A15	D12	I/O, TS	Address A15	20	X1-96
A16	C13	I/O, TS	Address A16	20	X1-95
A17	B13	I/O, TS	Address A17	20	X1-94
A18	D9	I/O, TS	Address A18	10	X1-93
A19	D11	I/O, TS	Address A19	20	X1-92
A20	C12	I/O, TS	Address A20	10	X1-91
A21	B12	I/O, TS	Address A21	10	X1-90
A22	B10	I/O, TS	Address A22	≈ 5	X1-89
A23	B11	I/O, TS	Address A23	≈ 5	X1-88
A24	C11	I/O, TS	Address A24	5	X1-87
A25	D10	I/O, TS	Address A25	5	X1-86
A26	C10	I/O, TS	Address A26	5	X1-85
A27	A13	I/O, TS	Address A27	5	X1-84
A28	A10	I/O, TS	Address A28	5	X1-83
A29	A12	I/O, TS	Address A29	5	X1-82

Specification TQM860M

Signal	No. of Pins	Type	Description	Ext. Load Cap. max. [pF]	Module Pin
A30	A11	I/O, TS	Address A30	45	X1-81
A31	A9	I/O, TS	Address A31 (LSB)	45	X1-80

Data Bus

D0	W14	I/O, TS	Data D0 (MSB)	9	X2-88
D1	W12	I/O, TS	Data D1	≈ 5	X2-89
D2	W11	I/O, TS	Data D2	9	X2-90
D3	W10	I/O, TS	Data D3	9	X2-91
D4	W13	I/O, TS	Data D4	9	X2-92
D5	W9	I/O, TS	Data D5	9	X2-93
D6	W7	I/O, TS	Data D6	9	X2-94
D7	W6	I/O, TS	Data D7	≈ 5	X2-95
D8	U13	I/O, TS	Data D8	25	X2-96
D9	T11	I/O, TS	Data D9	25	X2-97
D10	V11	I/O, TS	Data D10	25	X2-98
D11	U11	I/O, TS	Data D11	30	X2-99
D12	T13	I/O, TS	Data D12	25	X2-100
D13	V13	I/O, TS	Data D13	30	X2-101
D14	V10	I/O, TS	Data D14	25	X2-102
D15	T10	I/O, TS	Data D15	30	X2-103
D16	U10	I/O, TS	Data D16	30	X2-104
D17	T12	I/O, TS	Data D17	30	X2-105
D18	V9	I/O, TS	Data D18	30	X2-106
D19	U9	I/O, TS	Data D19	30	X2-107
D20	V8	I/O, TS	Data D20	30	X2-108
D21	U8	I/O, TS	Data D21	30	X2-109
D22	T9	I/O, TS	Data D22	30	X2-110
D23	U12	I/O, TS	Data D23	30	X2-111
D24	V7	I/O, TS	Data D24	30	X2-112
D25	T8	I/O, TS	Data D25	30	X2-113
D26	U7	I/O, TS	Data D26	30	X2-114
D27	V12	I/O, TS	Data D27	30	X2-115
D28	V6	I/O, TS	Data D28	30	X2-116
D29	W5	I/O, TS	Data D29	30	X2-117
D30	U6	I/O, TS	Data D30	30	X2-118
D31	T7	I/O, TS	Data D31 (LSB)	30	X2-119

Bus Control

IRQ0#	V14	I	Interrupt Request 0 (NMI), Pull-Up 4k7	50	X1-2
IRQ1#	U14	I	Interrupt Request 1, Pull-Up 4k7	50	X1-3
IRQ2#/RSV#	H3	I/O; TS	Interrupt Request 2 / Reservation, Pull-Up 4k7	50	X1-4
IRQ3#	V3	I	Interrupt Request 3, Pull-Up 4k7	50	X1-5
IRQ_CAN#/ IRQ4#	V5	I	Interrupt Request 4, used for CAN Interrupt, connected to P2.6/INT# of both AS82527 devices, Pull-Up 4k7	35	X1-6
IRQ5#	W4	I	Interrupt Request 5, Pull-Up 4k7	50	X1-7
IRQ6#	V4	I	Interrupt Request 6, Pull-Up 4k7	50	X1-8
IRQ7#	W15	I	Interrupt Request 7, Pull-Up 4k7	50	X1-9
RD/WR#	B2	I/O, TS	Read / Write	50	X2-73

Specification TQM860M

Signal	No. of Pins	Type	Description	Ext. Load Cap. max. [pF]	Module Pin
BB#	E1	I/O, TS	Bus Busy, Pull-Up 2k2	50	X2-75
BG#	E2	I/O	Bus Grant	50	X2-74
BR#	G4	I/O	Bus Request, Pull-Up 4k7	50	X2-76
BURST#	F1	I/O, TS	Burst Transaction	50	X2-82
BDIP#/GPL_B5#	D2	I/O, TS	Burst Data In Progress / General Purpose Line B5	50	X1-63
BI#	E3	I/O, TS	Burst Inhibit, Pull-Up 4k7	50	X2-81
TS#	F3	I/O, TS	Transfer Start, Pull-Up 4k7	50	X2-83
TA#	C2	I/O, TS	Transfer Acknowledge, Pull-Up 2k2	50	X2-77
TEA#	D1	I/O, OD	Transfer Error Acknowledge, Pull-Up 2k2	50	X2-80
TSIZ0/REG#	B9	I/O, TS	Transfer Size 0 / Register	50	X2-78
TSIZ1	C9	I/O, TS	Transfer Size 1	50	X2-79
IRQ4#/KR#/RETRY#	K1	I/O, TS	Interrupt Request 4 / Kill Reservation / Retry, Pull-Up 4k7	50	X2-72
CR#/IRQ3#	F2	I	Cancel Reservation / Interrupt Request 3	50	X2-70

Memory Controller

BS_A0#	D8	O	Byte Select A0	45	X1-56
BS_A1#	C8	O	Byte Select A1	45	X1-57
BS_A2#	A7	O	Byte Select A2	45	X1-58
BS_A3#	B8	O	Byte Select A3	45	X1-59
WE0#/BS_B0#	C7	O	Byte Select A0 / Write Enable 0	50	X1-76
WE1#/BS_B1#	A6	O	Byte Select A1 / Write Enable 1	50	X1-77
WE2#/BS_B2#	B6	O	Byte Select A2 / Write Enable 2	50	X1-78
WE3#/BS_B3#	A5	O	Byte Select A3 / Write Enable 3	50	X1-79
CS_FLASH0#/CS0#	C3	O	Chip Select 0 (Flash, Boot Chip Select)	35	X1-71
CS_FLASH1#/CS1#	A2	O	Chip Select 1 (Flash)	35	X1-70
CS_SDRAM0#/CS2#	D4	O	Chip Select 2 (SDRAM)	40	X1-69
CS_CAN#/CS3#	E4	O	Chip Select 3 (CAN)	40	X1-68
CS4#	A4	O	Chip Select 4	50	X1-67
CS5#	B4	O	Chip Select 5	50	X1-66
CS6#/CE1_B#	D5	O	Chip Select 6 / Card Enable 1 Slot B	50	X1-65
CS7#/CE2_B#	C4	O	Chip Select 7 / Card Enable 2 Slot B	50	X1-64
CE1_A#	B3	O	Card Enable 1 Slot A	50	X1-54
CE2_A#	A3	O	Card Enable 2 Slot A	50	X1-55
OE#/GPL_AB1#	C6	O	Output Enable / General Purpose Line A1 / B1, used for SDRAM and FLASH	10	X1-73
GPL_AB2#	B5	O	General Purpose Line A2 / B2, used for SDRAM and CAN	30	X1-74
GPL_AB3#	C5	O	General Purpose Line A3 / B3, used for SDRAM	40	X1-75
GPL_AB0#	D7	O	General Purpose Line A0 / B0	40	X1-72
UPWAITA/ GPL_A4#	C1	I/O	UPM Wait A / General Purpose Line A4,	50	X1-60
UPWAITB/ GPL_B4#	B1	I/O	UPM Wait B / General Purpose Line B4 used for CAN, Pull-Up 4k7	30	X1-61

Specification TQM860M

Signal	No. of Pins	Type	Description	Ext. Load Cap. max. [pF]	Module Pin
GPL_A5#	D3	O	General Purpose Line A5, used for CAN	45	X1-62
AS#	L3	I	Address Strobe, Pull-Up 4k7	50	X2-69
BADDR28	M3	O	Burst Address 28	50	X2-68
BADDR29	M2	O	Burst Address 29	50	X2-67
BADDR30/REG#	K4	O	Burst Address 30 / Register	50	X2-66

PCMCIA

WAIT_A#	R3	I	Wait Slot A, Pull-Up 4k7	50	X1-10
ALE_A	K2	O	Address Latch Enable A, Pull-Up 4k7	50	X1-11
IP_A0	T5	I	Input Port A0, Pull-Up 4k7	50	X1-12
IP_A1	T4	I	Input Port A1, Pull-Up 4k7	50	X1-13
IP_A2	U3	I	Input Port A2, Pull-Up 4k7	50	X1-14
IP_A3	W2	I	Input Port A3, Pull-Up 4k7	50	X1-15
IP_A4	U4	I	Input Port A4, Pull-Up 4k7	50	X1-16
IP_A5	U5	I	Input Port A5, Pull-Up 4k7	50	X1-17
IP_A6	T6	I	Input Port A6, Pull-Up 4k7	50	X1-18
IP_A7	T3	I	Input Port A7, Pull-Up 4k7	50	X1-19
WAIT_B#	R4	I	Wait Slot B, Pull-Up 4k7	50	X1-24
ALE_B	J1	O	Address Latch Enable B, Pull-Up 4k7	50	X1-25
IP_B0/VFLS0	H2	I	Input Port B0 / CPU history buffer status 0, Pull-Up 4k7	50	X1-33
IP_B1/VFLS1	J3	I	Input Port B1 / CPU history buffer status 1, Pull-Up 4k7	50	X1-32
IP_B2	J2	I	Input Port B2, Pull-Up 4k7	50	X1-31
IP_B3	G1	I	Input Port B3, Pull-Up 4k7	50	X1-30
IP_B4	G2	I	Input Port B4, Pull-Up 4k7	50	X1-29
IP_B5	J4	I	Input Port B5, Pull-Up 4k7	50	X1-28
IP_B6	K3	I	Input Port B6, Pull-Up 4k7	50	X1-27
IP_B7	H1	I	Input Port B7, Pull-Up 4k7	50	X1-26
OP0	L4	O	Output Port 0	50	X1-21
OP1	L2	O	Output Port 1	50	X1-20
OP2/MODCK1	L1	I/O	Output Port 2 / Mode Clock 1	45	X1-22
OP3/MODCK2	M4	I/O	Output Port 3 / Mode Clock 2	45	X1-23

Other CPU Signals

SPARE1/ MII_CR_S	B7	I	MII Carrier Receive Sense / Spare 1	50	X2-87
SPARE2/ MII_MDIO	H18	I/O	MII Management Data / Spare 2	50	X2-86
SPARE3/ MII_TX_EN	V15	O	MII Transmit Enable / Spare 3	50	X2-85
SPARE4/ MII_COL	H4	I	MII Collision / Spare 4	50	X2-84
CLKOUT	W3	O	Clock Out	30	X1-40
EXTCLK	N2	I	External Clock	50	X1-39
TEXP	N3	O	Timer Expired	50	X1-36
PORESET#	R2	O	Power-On Reset, connected to Voltage Supervisor output (3.3 and 5 V)	50	X1-35
HRESET#	N4	I/O, OD	Hard Reset, Pull-Up 1k	50	X1-37
SRESET#	P2	I/O, OD	Soft Reset, Pull-Up 10 k, LED with 220 Ω to VCC3V3	50	X1-42

Specification TQM860M

Signal	No. of Pins	Type	Description	Ext. Load Cap. max. [pF]	Module Pin
RSTCONF#	P3	I	Reset Configuration, Pull-Down 1 k	50	X1-38
DSDI/TDI	H17	I	Development Serial Data In / Test Data In	50	X2-44
DSDO/TDO	G17	O	Development Serial Data Out / Test Data Out	50	X2-45
DSCK/TCK	H16	I	Development Serial Clock / Test Clock, Pull-Down 1k	50	X2-46
TMS	G18	I	Test Mode Select, Pull-Up 10 k	50	X2-47
FRZ/IRQ6#	G3	I/O	Freeze / Interrupt Request 6, Pull-Up 4k7	50	X2-71

Port A

PA0	U19	I/O	Port A0	50	X2-28
PA1	T19	I/O	Port A1	50	X2-29
PA2	R18	I/O	Port A2	50	X2-30
PA3	P17	I/O	Port A3	50	X2-31
PA4	P19	I/O	Port A4	50	X2-32
PA5	N18	I/O	Port A5	50	X2-33
PA6	M17	I/O	Port A6	50	X2-34
PA7	M19	I/O	Port A7	50	X2-35
PA8	L17	I/O	Port A8	50	X2-36
PA9	K18	I/O	Port A9	50	X2-37
PA10	J17	I/O	Port A10	50	X2-38
PA11	G16	I/O	Port A11	50	X2-39
PA12	F17	I/O	Port A12	50	X2-40
PA13	E17	I/O	Port A13	50	X2-41
PA14	D17	I/O	Port A14	50	X2-42
PA15	C18	I/O	Port A15 (via analog switch)	~ 10	X2-43

Port B

PB14	U18	I/O	Port B14	50	X2-48
PB15	R17	I/O	Port B15	50	X2-49
PB16	N16	I/O	Port B16	50	X2-50
PB17	P18	I/O	Port B17	50	X2-51
PB18	N17	I/O	Port B18	50	X2-52
PB19	N19	I/O	Port B19	50	X2-53
PB20/SMRXD2#	L16	I/O	Port B20, used as SMRXD2#, connected to RS232-Driver TTL-Output via 4k7 resistor to allow other usage	50	X2-54
PB21/SMTXD2#	K16	I/O	Port B21, used as SMTXD2#, connected to RS232-Driver TTL-Input	50	X2-55
PB22	L19	I/O	Port B22	50	X2-56
PB23	K17	I/O	Port B23	50	X2-57
PB24/SMRXD1# RXD3#	J18	I/O	Port B24, used as SMRXD1# or RXD3#, connected to RS232-Driver TTL-Output via 4k7 resistor to allow other usage	50	X2-58
PB25/SMTXD1#/ TXD3#	J16	I/O	Port B25, used as SMTXD1# or TXD3#, connected to RS232-Driver TTL-Input	50	X2-59
PB26/I2CSCL	F19	I/O	Port B26, used as I2CSCL, connected to serial EEPROM, pull-up 4k7	44	X2-60
PB27/I2CSDA	E19	I/O	Port B27, used as I2CSDA, connected to serial EEPROM, pull-up 4k7	42	X2-61
PB28	D19	I/O	Port B28	50	X2-62

Specification TQM860M

Signal	No. of Pins	Type	Description	Ext. Load Cap. max. [pF]	Module Pin
PB29	E16	I/O	Port B29	50	X2-63
PB30	C19	I/O	Port B30	50	X2-64
PB31	C17	I/O	Port B31	50	X2-65

Port C

PC4	T17	I/O	Port C4	50	X2-16
PC5	T18	I/O	Port C5	50	X2-17
PC6	R19	I/O	Port C6	50	X2-18
PC7	M16	I/O	Port C7	50	X2-19
PC8	M18	I/O	Port C8	50	X2-20
PC9	L18	I/O	Port C9	50	X2-21
PC10	K19	I/O	Port C10	50	X2-22
PC11	J19	I/O	Port C11	50	X2-23
PC12	F18	I/O	Port C12	50	X2-24
PC13	E18	I/O	Port C13	50	X2-25
PC14	D18	I/O	Port C14	50	X2-26
PC15	D18	I/O	Port C15	50	X2-27

Port D

PD3	W16	I/O	Port D3	50	X2-3
PD4	U16	I/O	Port D4	50	X2-4
PD5	U15	I/O	Port D5	50	X2-5
PD6	V16	I/O	Port D6	50	X2-6
PD7	T15	I/O	Port D7	50	X2-7
PD8	W17	I/O	Port D8	50	X2-8
PD9	V17	I/O	Port D9	50	X2-9
PD10	W18	I/O	Port D10	50	X2-10
PD11	T16	I/O	Port D11	50	X2-11
PD12	R16	I/O	Port D12	50	X2-12
PD13	V18	I/O	Port D13	50	X2-13
PD14	V19	I/O	Port D14	50	X2-14
PD15	U17	I/O	Port D15	50	X2-15

Signal	No. of Pins	Type	Description	Ext. Load Cap. max. [pF]	Module Pin
--------	-------------	------	-------------	--------------------------	------------

Non-CPU Signals

RESIN#	1	I	Reset Input (Master Reset Input of Voltage Supervisor), Pull-Up 4k7	–	X1-34
HRESETF#	1	I	Flash Reset Signal (12 V may be applied without damaging the module – however, this is not recommended)	–	X1-44
ENMON#	1	I	Monitor Enable (enables MON8xx interactive Mode), Pull-Up 10 k	–	X1-41
CKE	1	I	SDRAM Clock Enable, Pull-Up 4k7	–	X1-45
JTAG/BDM#	1	I	JTAG / BDM Configuration (via Hard Reset Configuration), Pull-Up 10 k	–	X1-43
SMRXD1	1	I	SMC1 Receive Data, RS232 level	–	X1-52

Specification TQM860M

Signal	No. of Pins	Type	Description	Ext. Load Cap. max. [pF]	Module Pin
SMTXD1	1	O	SMC1 Transmit Data, RS232 level	1000 3 kΩ	X1-53
SMRXD2	1	I	SMC2 Receive Data, RS232 level	–	X1-50
SMTXD2	1	O	SMC2 Transmit Data, RS232 level	1000 3 kΩ	X1-51
RX0_CAN1	1	I	CAN controller 1 RX0	–	X1-49
TX0_CAN1	1	O	CAN controller 1 TX0	50	X1-48
RX0_CAN2	1	I	CAN controller 2 RX0	–	X1-47
TX0_CAN2	1	O	CAN controller 2 TX0	50	X1-46

Power Supply

VCC5V	3	V	5 V Supply (CAN Controller, switching regulator input)	–	X1-116 X1-118 X1-120
VCC3V3	3	V	3.3 V Supply (switching regulator output)	–	X1-112 X1-113 X1-114
VBAT	1	V	Battery Voltage, connected via Schottky Diode and RC-Combination (1 kΩ / 100 nF) to KAPWR	–	X2-1
DGND	6	V	(Digital) Ground	–	X1-1 X1-115 X1-117 X1-119 X2-2 X2-120

Table 22: Module connector pinout

For connecting the supply voltage see 3.2.

3.4 Mechanics Specification

3.4.1 General Information

- Double-row, multipolar 0.8 mm pitch SMD connector 2 * 120pole
- The combination with various counterparts allows different mounting heights to be able to adapt to the assembly of the mainboard.
- Double-sided SMD fitting
- 8-layer multilayer in Micro-Via technology

3.4.2 Dimensions

- Board dimensions 54 mm * 44 mm
- Mounting height: a + b + c = 10.6 mm
- Free mounting height under module: a – d = 2.6 mm (see Figure 12)

Specification TQM860M

The shaded areas drawn in the following figure should be kept free in the base board for the extractor tool MOZI8xxL. The shaded areas are symmetrical. The drawing shows the position of the tool in mounted state (right) and during mounting (left).

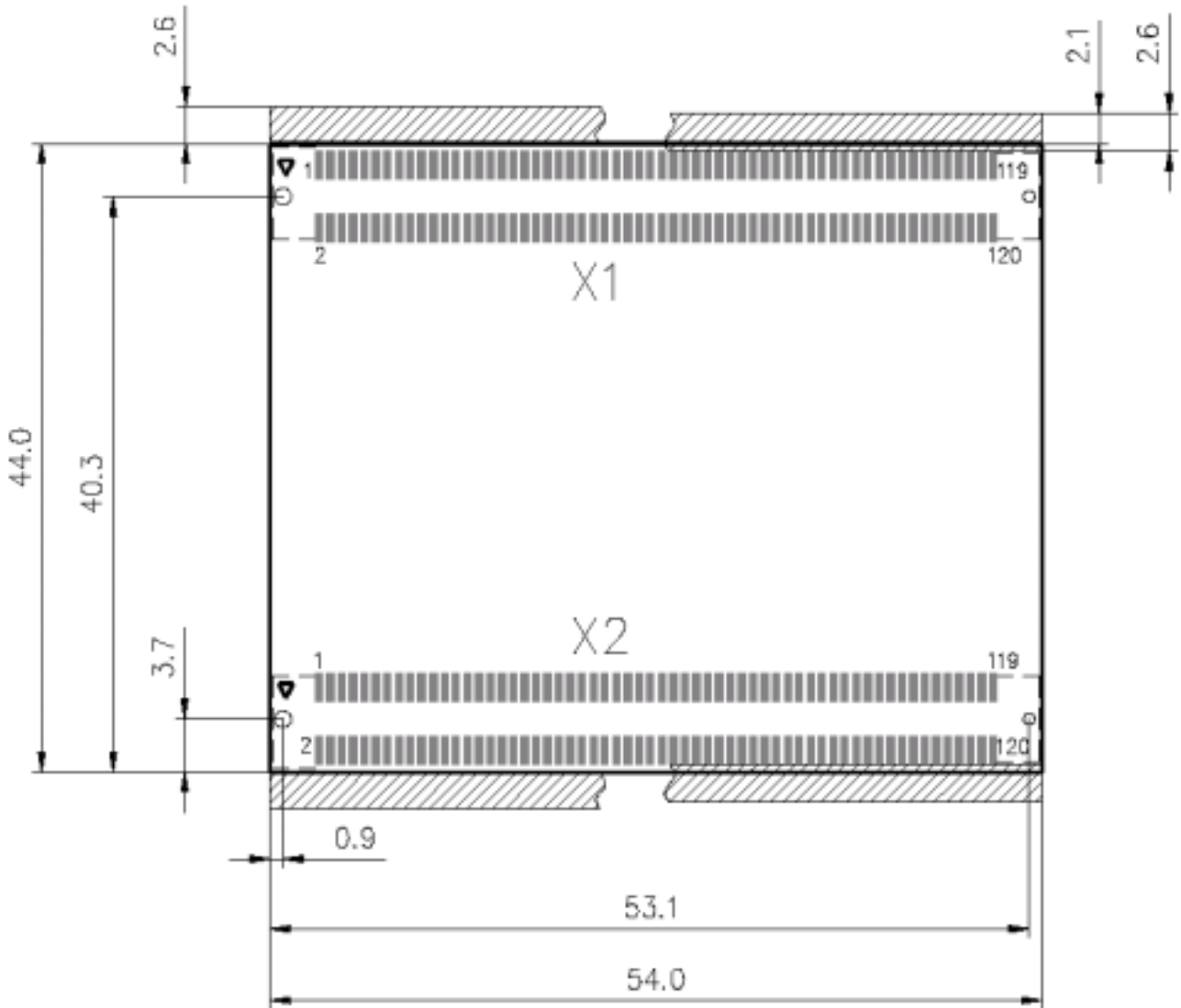


Figure 11: View from top through board

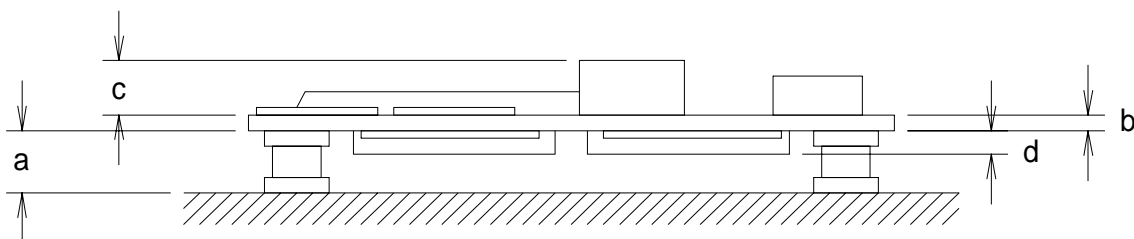


Figure 12: Mounting Heights (not to scale)

Specification TQM860M

Measure	Value [mm]	Comment
a	5.0 +0.4 / -0.3	Combination of module connector with counterpart; with different connector on base board also 6, 7 and 8 mm possible
b	1.5 ± 0.15	Board
c	3.5 ± 0.5	Power inductor [16] (max. mounting height upper side)
d	2.35 max.	CAN controller [13] (max. mounting height bottom side)

Table 23: Mounting Heights

3.4.3 Connector

Board-to-Board Distance	Module				Base Board Connector		
	No. of Pins	Qty	Supplier	Order No.	No. of Pins	Supplier	Order No.
5 mm	120	2	AMP Berg	177983-5 61082-121000	120	AMP Berg	177984-5 61083-121000
6 mm					120	AMP Berg	5-179029-5 61083-122000
7 mm					120	AMP Berg	5-179030-5 61083-123000
8 mm					120	AMP Berg	5-179031-5 61083-124000

Table 24: Connector types

3.4.4 Handling

To carefully remove the module from base boards, the use of the extractor tool MOZI8xxL included in the starter kit is recommended.

3.5 Monitor Software

The monitor program MON8xx is delivered with TQM8xxM and TQM8xxL modules as default software. After connecting a serial interface and the supply voltage, and in combination with a starter kit STK8xxL, it enables the communication with the module. The MON8xx provides the basic functionality for putting the TQM8xxL into operation. This functionality includes:

- Monitor functions:
Memory and register monitor for addressing the memory and registers of the MPC8xx, as well as further – also external – memory mapped I/Os. Simple I/O functions like edit memory, dump, change register, or the possibility to load S-record files into the RAM of flash.
- Automatic application start:
After a reset, you can either start the monitor or an application / an operating system. When the MON8xx is started, it addresses the port pin led onto the debugging interface (signal ENMON#) and either branches off to the monitor or starts an application or operating system.

The specification of the MON8xx is contained in a separate document.

NOTE:

Due to different sector alignment the flash types AM29DL163DB and AM29LV320MB are not supported by the current MON8xx monitor version 110 (see also section 3.1.10).

3.6 Safety Requirements and Protective Provisions

3.6.1 EMC Requirements

For CE certification the following standards have to be met:

- EN 50081-1: Emission of EMC disturbances in residential environment
- EN 50082-2: Immunity from EMC disturbances in industrial environment

These standards have to be met in the context of a reference design. In this case, the reference design is the starter kit STK8xxL.

The module was carefully developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, however, anti-interference measures may become necessary in order to safeguard that the entire system keeps to certain limits.

The following measures are recommended:

- Stable ground conditions (sufficient ground areas) on the board
- For metal housings, a good (at least HF) connection of the board grounding to the housing potential
- Sufficient bypass capacitors for all supply voltages
- Keep fast or continuously pulsing lines short (e.g. clock); avoid interference with other signals by keeping distance and / or shielding
- Filtering of all signals that can be connected externally ("slow" and DC signals can also emit HF indirectly)

3.6.2 ESD Requirements

To avoid coupling the ESD pulse into the system on the way from the input to the protective circuit, protection against electrostatic discharge is most sensibly provided directly at the input of a system. Since these measures always have to be realized on the base board, no specific protection circuitry was included on the module. The used components themselves offer a certain protection according to their specification, which however, is generally not sufficient to meet the legal requirements.

The following measures are recommended:

- Generally: Shielding of the feed lines (shielding on both sides solidly connected to ground / housing)
- For supply voltages: Protection by suppressor diode(s)
- Slow signal lines: RC filtering, possibly Z-diode
- Fast signal lines: Integrated protective modules (suppressor diode arrays)

3.6.3 Operating Safety

A separate test is not necessary due to the voltages applied (≤ 5 V DC).

3.7 Environmental Conditions

3.7.1 Climate and Operative Range

- Ambient temperature : 0 °C .. 70 °C, optionally –40 °C .. +85 °C
- Storage temperature : –20 °C .. +100 °C
- Protection class: : IP00 (no protection against solid bodies and liquids)

3.7.2 Mounting Conditions

The critical component with respect to heating is the CPU. In still air (natural convection possible), operation within the whole ambient temperature range without cooling measures is possible. When mounting the module, please observe the following:

- Inside a closed housing, a rise in temperature generally occurs. The relevant factor with regard to operating safety is the ambient temperature of the module, so that the admissible maximum temperature for the entire device must be reduced. An improvement can be achieved e.g. by direct thermal connection of the module (heat conducting cellular plastic / rubber) to a cooling surface or by ventilation.
- Inside closed housings, heating of the module by other sources of heat may occur. Remedy as above, or by insulating the source(s) of heat.

3.8 Reliability and Useful Life

For the module, a FIT rate of $800 * 10^{-9} / h$ was calculated [19].

At least 100 insertion / withdrawal cycles are guaranteed for the connectors used [18].

3.9 Product Qualification

For a product qualification, the modules were tested or are being prepared to be tested according to the following standards:

3.9.1 Mechanical Strain

Vibration	EN 60068-2-6
Shock	EN 60068-2-27

3.9.2 Temperature Tests

Thermal shock	EN 60068-2-14
Cold storage	EN 60068-2-1
Dry heat storage	EN 60068-2-2
Damp heat storage	DIN IEC 68-2-3

3.9.3 EMC

Generic emission standard, Part 1: Residential, commercial and light industry EN 50081

3.9.4 EMC Immunity

Generic immunity standard, Part 2: Industrial environment EN 50082

3.9.5 ESD

Generic immunity standard, Part 2: Industrial environment EN 50082

3.9.6 UL Approval

An UL certification can be obtained if required.

4. Appendix

4.1 References

- [1] MPC860 PowerQUICC™ User's Manual
MPC860UM/AD Rev. 1, Motorola Inc. 07/98
- [2] Errata to MPC860 PowerQUICC™ User 's Manual Rev.1
MPC860UMAD/D, Rev.2, Motorola Inc. 6/2001
- [3] MPC855T User's Manual
Integrated Communications Microprocessor
MPC855TUM/D Rev. 0, Motorola Inc. 2/2001
- [4] MPC866 PowerQUICC™ Family User's Manual
MPC866UM/D Rev. 1.1, Motorola Inc. 05/2003
- [5] MPC860 Family Hardware Specifications
MPC860EC/D Rev. 6.0, Motorola Inc. 10/2002
- [6] MPC862/857T/857DSL Hardware Specifications
MPC862EC/D Rev. 1, Motorola Inc. 9/2002
- [7] MPC866/859 Hardware Specifications
MPC866EC/D Rev. 1.3, Motorola Inc. 05/2003
- [8] AM29LV160D
16 Megabit (2 M x 8-Bit/1 M x 16-Bit) CMOS 3.0 Volt-only Boot Sector Flash Memory
Publication #22358 Rev. A Amendment /+1, Issue Date April 19, 1999
- [9] 256 MB: x4, x8, x16 SDRAM
256MSDRAM_C.p65 – Rev. C; Pub. 4/01
- [10] M24C64, M24C32 64/32 Kbit Serial I²C Bus EEPROM
STMicroelectronics, 01/2002
- [11] AT24C128, AT24C256 2-Wire Serial CMOS E²PROM 128K (16,384 x 8), 256K (32,768 x 8)
Rev. 0670F–SEEPR–2/02
- [12] 82527 Serial Communications Controller
Controller Area Network Protocol
Order Number 272250-006, December 1995
- [13] Intel 1999 Packaging Databook
- [14] MAX3222/MAX3232/MAX3237/MAX3241
3.0V to 5.5V, Low-Power, up to 1Mbps, True RS-232 Transceivers Using Four 0.1µF External
Capacitors
19-0273; Rev 5; 3/99
- [15] MAX814/MAX815/MAX816
±1 % Accuracy, Low-Power, +3V and +5V µP Supervisory Circuits
19-0412, Rev 0, 6/95

Specification TQM860M

- [16] SN74AVC16835 18-Bit Universal Bus Driver with 3-State Outputs
SCES168J – Texas Instruments Inc., December 1995 – Revised February 2002
- [17] Anla Technology Co., Ltd.
EMC EMI Component SMD
- [18] Product Specification 108-5390
AMP FH 0.8 mm Pitch Board-to-Board Connector
AMP J-552 (Rev. Mar 91)
- [19] Lebensdauer- und Zuverlässigkeitsberechnung
Arbeitsanweisung QMAA0704A05 Rev. 109, TQ-Systems GmbH
- [20] MPC860 Family Hardware Specifications
MPC860EC/D Rev. 5.1, 11/2001
- [21] MAX1626/MAX1627
5V/3.3V or Adjustable, 100% Duty-Cycle, High-Efficiency, Step-Down DC-DC Controllers
19-1075; Rev 0; 6/96
- [22] MON8xx.SZ.110
Spezifikation MON8xx
Rev 110; TQ-Systems GmbH, 28/07/2003

4.2 Configuration of SDRAMs

The UPM configuration for the SDRAMs can be found in the Startup Code of the monitor program MON8xx (file STARTUP.S, see [22])

4.3 Configuration of the CAN controllers

The UPM configuration for the CAN controllers can be found in the monitor program MON8xx (files CAN.C, CAN.H, see [22]).

Note regarding handling and archiving

The current revision of the specification is stored on the server in the current project directory in the subdirectory DOC under the name TQM860M.SZ.XXX.DOC. The individual revisions of the specification are stored as annex to the Review form in the development folder.